An Analytic Approach to Optimum Oscillator Design Using *S*-Parameters

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Abstract—**An analytic approach to the design of microwave FET oscillators for maximum power output into a given load is presented. By the use of FET *S*-parameters, characterized as a function of incident input powers, design information can be obtained for any standard topology. By means of this technique, an experimental 5.3-GHz oscillator has been demonstrated which delivers 245 mW at 35-percent efficiency into a 50-Ω load.**

I. Introduction

MONOLITHIC microwave integrated circuits may require the implementation of GaAs MESFET oscillators, particularly in receiver applications. Such oscillators have good output power and stability along with the advantage of easy integration. However, their design is complicated by the fact that MESFET's are two-port devices rather than one-port devices such as Gunn or IMPATT diodes.

Current approaches to oscillator design with active two-ports typically involve reduction to a one-port configuration by embedding the device in a suitable circuit. The circuit topology is usually chosen to resonate the input port so that the stability factor is less than unity at the frequency of operation; an output load circuit is then designed to match the resulting negative output impedance. While yielding practical oscillators, this approach gives no information about the output impedance needed to obtain maximum power.

Maeda *et al.* [1] postulate that the optimum power will be obtained when the real part of the output impedance (of the resultant one-port network) is at its maximum value, but no simple approach exists to design the embedding circuit in order to achieve this. Rauscher [2] has investigated oscillator design using a nonlinear time-domain model for the FET. His method involves analytic determination of the transistor drain and gate voltage, and load impedance at the point of maximum power, using parameters obtained from the model.

Oscillator design requires a means of characterizing the nonlinear active element as well as a procedure to synthesize the external linear circuit to meet the design specifications. Large-signal scattering parameters provide a convenient way of representing the device. This paper presents a systematic approach to oscillator design using large-signal *S*-parameters [3], [4].

Vehovec *et al.* [5] investigated maximum power design using large-signal *Y*-parameters which are functions of a single port voltage. Kotzebue and Parrish [6] reformulated that work and obtained equations for the external network elements, in terms of the device *Y*-parameters, for each of the six basic oscillator topologies. This approach was later used by Johnson [7] who applied the results to the design of a microwave FET oscillator. However, he used measured large-signal *S*-parameters, which were then converted mathematically to *Y*-parameters. Such conversion need not give the correct *Y*-parameters in a large-signal nonlinear system.

Y- and *S*-parameters give representations of linear circuit elements. Since the MESFET is a nonlinear device, its behavior must first be linearized about its in-circuit operating level if *S*-parameters are to be sensibly applied. Such quasi-linearization is useful in the design stage only if the terminal conditions used to determine the parameter matrix reflect those that are present in actual operation. Consequently, it is necessary to characterize the device with a matrix set consistent with the design method, if the device is nonlinear.

The technique presented here is based on *S*-parameters, which either may be measured under high drive conditions [7], or obtained through the use of a model. A nonlinear representation of the FET with its parasitic circuit elements has been reported [8], and is used here. The device response is predicted for variable drive conditions. From this, the *S*-parameters can be calculated at any power level.

Inherent in quasi-linearization using *S*-parameters are the following assumptions:

a) Nearly sinusoidal voltages are present. The effect of harmonic voltages and their terminations are neglected.

b) The input *S*-parameters are functions only of the incident input power $|V_1^+|^2$, and the output *S*-parameters are functions only of the input power incident on the output port $|V_2^+|^2$. This assumption is a necessary condition for large-signal *S*-parameters to be defined, and is discussed in detail by Gilmore *et al.* [3].

Both these assumptions (as applied to large-signal *Y*-parameters) are inherent in the approach of Vehovec *et al.* [5].

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The approach presented here uses large-signal S-parameters and is novel in two respects.

1) It is readily applicable at microwave frequencies, and to GaAs MESFET's in particular, for which large-signal S-parameters can be directly measured.

2) It allows the easy extension of the device reference planes by transmission lines, and their incorporation into the design technique. This is often a necessary condition for physical realizability. These lengths can then be included in the optimization. Such treatment of transmission lines is considerably more difficult using Y-parameters.

The cost of these advantages is that no simple explicit formula can be derived for the external embedding elements. This is because the S-matrix for the embedding network contains higher order powers of the elements therein (whereas the Y-matrix is linear in the elements). The result is a set of nonlinear equations which must be solved for the element values. It should be noted, however, that the Y-parameter approach [2] will also become nonlinear if one seeks to extend the device reference planes by transmission lines (assuming one could measure the Y-parameters at microwave frequencies).

II. Oscillator Design with Specified Gain

Fig. 1 shows an oscillator comprising an active two-port device embedded in an external circuit. The active device is described by its large-signal S-parameters. The quantity $|V_1^+|^2$ is the power incident on port 1 of the device; $|V_2^+|^2$ is the power incident on port 2. The incident wave V_1^+ is fixed at the outset of the oscillator design to be equal to the amplitude used during measurement of S_{11} and S_{21}. It may be set at the point of maximum power added efficiency as described by Pucel [9] or Johnson [7], or through simulations as was done here. Similarly, V_2^+ is unknown at the outset. Its value should be initially estimated; its true value can be checked in the final design.

The complex voltage V_2^- is a free parameter. By defining the gain

$$A = \frac{V_2^-}{V_1^+} = A_R + jA_I$$

the power delivered to the external network can be maximized as a function of A.

For the active device embedded in its external network, the condition for oscillation is

$$\begin{aligned}(Z_{\text{in}})\text{device}|_1 &= -(Z_{\text{in}})\text{network}|_1 \\ (Z_{\text{in}})\text{device}|_2 &= -(Z_{\text{in}})\text{network}|_2 \end{aligned} \tag{1}$$

corresponding to the conditions

$$\begin{aligned} V_{1N}^+ &= V_1^- \quad \text{and} \quad V_{1N}^- = V_1^+ \\ V_{2N}^+ &= V_2^- \quad \text{and} \quad V_{2N}^- = V_2^+ . \end{aligned} \tag{2}$$

Here, $(Z_{\text{in}})\text{device}|_1$ is the device input impedance at port 1, and $(Z_{\text{in}})\text{network}|_1$ is the external embedding network input impedance at port 1. For example, port 1 might represent the gate of a common source FET, and port 2 the drain.

The device can be described in quasi-linear form by its large-signal S-parameters, each assumed to be a function of a single variable

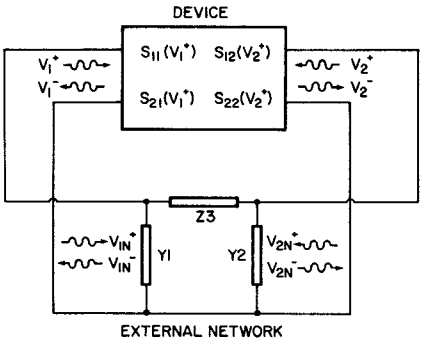

Fig. 1. Oscillator topology for a shunt embedding circuit. The device is represented by large-signal S-parameters. The incident and reflected voltage waves are shown.

$$V_1^- = S_{11}(|V_1^+|)V_1^+ + S_{12}(|V_2^+|)V_2^+ \tag{3a}$$

$$V_2^- = S_{21}(|V_1^+|)V_1^+ + S_{22}(|V_2^+|)V_2^+ . \tag{3b}$$

The linear embedding network may be described by inverse S-parameters, $\mathcal{S}^{-1}$, using (2)

$$V_1^- = \mathcal{S}_{11}^{-1}V_1^+ + \mathcal{S}_{12}^{-1}V_2^+ \tag{4a}$$

$$V_2^- = \mathcal{S}_{21}^{-1}V_1^+ + \mathcal{S}_{22}^{-1}V_2^+ . \tag{4b}$$

Substituting $V_2^- = AV_1^+$ into (3b) gives

$$V_2^+ = \left[\frac{A - S_{21}(|V_1^+|)}{S_{22}(|V_2^+|)}\right]V_1^+ . \tag{5}$$

Equating (3) and (4), and using (5) gives the design equations

$$S_{22}\mathcal{S}_{11}^{-1} + \mathcal{S}_{12}^{-1}(A - S_{21}) - S_{11}S_{22} + S_{12}S_{21} - AS_{21} = 0 \tag{6a}$$

$$S_{22}\mathcal{S}_{21}^{-1} + \mathcal{S}_{22}^{-1}(A - S_{21}) - AS_{22} = 0. \tag{6b}$$

This set of four equations (using real and imaginary parts) describes the condition for oscillation. Provided that A is suitably chosen so that the device generates power, the required network conditions are completely described by (6).

III. Determination of the Device S-Matrix and Network Inverse S-Matrix

The large-signal S-parameters of the device are just those measured or modeled. If desired, transmission lines of length θ_1 and θ_2 can be added at the gate and drain, respectively, to extend the reference planes of the device. The S-parameters are then

$$[S] = \begin{bmatrix} S_{11}e^{-j2\theta_1} & S_{12}e^{-j(\theta_1+\theta_2)} \\ S_{21}e^{-j(\theta_1+\theta_2)} & S_{22}e^{-j2\theta_2} \end{bmatrix} \tag{7}$$

where θ_1 and θ_2 can be chosen as variables.

The S-parameters of the linear network are found by cascading the transmission matrices of the three component elements, normalized to Z_0. In the example consid-

ered here, the external network is a pi- (shunt) topology, as shown in Fig. 1. The series oscillator, in which the external circuit has a T-topology, can be analyzed in the same way.

For the shunt network

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Y_1 & 1 \end{bmatrix} \begin{bmatrix} 1 & Z_3 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y_2 & 1 \end{bmatrix} = \begin{bmatrix} 1+Z_3Y_2 & Z_3 \\ Y_1+Y_2+Y_1Y_2Z_3 & 1+Y_1Z_3 \end{bmatrix}. \tag{8}$$

By conversion to the S-matrix and matrix inversion, the inverse S-matrix of the embedding pi-network is then

$$\mathcal{S}^{-1} = \frac{1}{(Y_1+Y_2)+Z_3(1-Y_2)(1-Y_1)-2} \begin{bmatrix} Z_3(1+Y_1)(1-Y_2)-(Y_1+Y_2) & -2 \\ -2 & Z_3(1-Y_1)(1+Y_2)-(Y_1+Y_2) \end{bmatrix}. \tag{9}$$

On substitution of S_{ij} and $\mathcal{S}_{ij}^{-1}$ into the four equations (6), four of the eight unknowns ($G_1 + jB_1, G_2 + jB_2, R_3 + jX_3, \theta_1, \theta_2$) are determined. By arbitrarily choosing the other four unknowns (such as by specifying the load impedance, taking the embedding elements reactive, and applying physical realizability constraints), the circuit can be optimized through choice of A, to deliver maximum power into the load. The circuit is found through solution of (6), using standard nonlinear root finding methods.

IV. Optimization of A for Maximum Power

Optimization of $A = V_2^-/V_1^+$, keeping V_1^+ constant, requires that V_2^- be varied in both magnitude and phase until the power delivered to the external network is a maximum. Referring to Fig. 1, the power delivered to the load is given by

$$\begin{aligned} P &= |V_1^-|^2 - |V_1^+|^2 + |V_2^-|^2 - |V_2^+|^2 \\ &= |V_1^+|^2 \left\{ |S_{11}|^2 + 2\,\mathrm{Re}\left(\frac{S_{11}^* S_{12}(A - S_{21})}{S_{22}} \right) + \left(\frac{|S_{12}|^2 - 1}{|S_{22}|^2} \right) \right. \\ &\quad \left. \cdot \left(|A - S_{21}|^2 \right) + |A|^2 - 1 \right\} \end{aligned} \tag{10}$$

which may be written

$$\begin{aligned} P = |V_1^+|^2 \Bigg\{ & |S_{11}|^2 + \frac{S_{11}S_{12}^*}{S_{22}^*}(A_R - jA_I - S_{21}^*) \\ & + \frac{S_{12}S_{11}^*}{S_{22}}(A_R + jA_I - S_{21}) + A_R^2 + A_I^2 - 1 \\ & + \frac{|S_{12}|^2 - 1}{|S_{22}|^2}\left(A_R^2 - A_R S_{21}^* + A_I^2 - jA_I S_{21}^* - A_R S_{21} + jA_I S_{21} + |S_{21}|^2 \right) \Bigg\}. \end{aligned} \tag{11}$$

The power has a local turning point at $\partial P/\partial A_R = 0$, and $\partial P/\partial A_I = 0$, giving

$$\mathrm{Re}\left[\frac{S_{12}^* S_{11}}{S_{22}^*} \right] + A_R \left[1 + \frac{|S_{12}|^2 - 1}{|S_{22}|^2} \right] - \left[\frac{|S_{12}|^2 - 1}{|S_{22}|^2} \right] \mathrm{Re}\, S_{21} = 0 \tag{12a}$$

$$\mathrm{Im}\left[\frac{S_{12}^* S_{11}}{S_{22}^*} \right] + A_I \left[1 + \frac{|S_{12}|^2 - 1}{|S_{22}|^2} \right] - \left[\frac{|S_{12}|^2 - 1}{|S_{22}|^2} \right] \mathrm{Im}\, S_{21} = 0 \tag{12b}$$

so that

$$A_{\mathrm{opt}} = \frac{1}{|S_{22}|^2 + |S_{12}|^2 - 1}\left(|S_{12}|^2 S_{21} - S_{21} - S_{22} S_{11} S_{12}^* \right). \tag{13}$$

Now, P is a maximum if the second derivatives are negative, which is true if $|S_{12}|^2 + |S_{22}|^2 < 1$. This condition will almost always be satisfied for the FET.

It will be noted in (13) on substituting for S from (7), that the magnitude of A_{opt} is independent of the line lengths θ_1 or θ_2. Similarly, the coefficient of V_1^+ in (5) and of $|V_1^+|^2$ in (10) is unchanged by the addition of lengths of line on either side of the transistor. Thus, for a given device, the optimum gain and power out is set solely by the FET S-parameters. As would be expected intuitively, the line lengths serve only as impedance transformers.

With A_{opt} so determined, one can generate, using (6), an infinite number of realizations with G_1, G_2, and R_3 positive. However, the three usual shunt topologies are those in which only one of G_1, G_2, or R_3 is nonzero, so that the load is confined to one element only. The case where the load is connected to port 2 (i.e., $G_1 = R_3 = 0$, $G_2 = 1$) is given as an example below.

The situation may arise where there are more than four degrees of freedom, i.e., insufficient constraints. No additional power may be obtained through use of these additional degrees of freedom, however, since the maximum power out in (10) is a function only of the FET S-parameters. The condition for oscillation given by (6) effectively reduces by four the total number of variables. Any degrees of freedom remaining beyond this cannot be further optimized to maximize output power; however, the degrees of freedom may influence other oscillator properties such as noise, stability, spectral purity, and tunable bandwidth. For instance, the device-network impedance crossing angle (as defined by Kurokawa [10]) could be set by the remaining variables to adjust these characteristics.

V. Oscillator Design Example

As an example of the method, consider the design of an FET oscillator which delivers maximum power into a 50-Ω load. For reactive embedding elements ($G_1 = R_3 = 0$) and $Y_2 = 1$, the unknown quantities are θ_1, θ_2, B_1, and X_3. Such

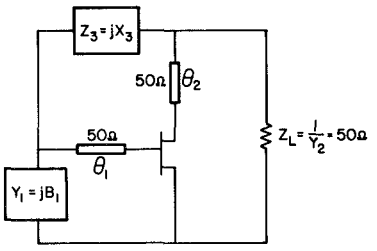

Fig. 2. Generalized oscillator circuit for the design example given.

a case is completely constrained and is illustrated in Fig. 2.

This design is practical from the viewpoint of a carrier mounted FET with external feedback, in which the feedback points are movable. Note, further, that no output load transformer is required, since Y_2 is specified directly to represent 50 Ω. A short computer program was written to calculate the device S-parameters for assumed values of θ_1 and θ_2 using (7), and the network inverse S-matrix for assumed values of B_1 and X_3 using (9). These values were then substituted into (6), and the equations solved using a standard quasi-Newton routine, as a function of the variables θ_1, θ_2, B_1, and X_3.

From the viewpoint of implementation, it is easiest to treat the feedback element Z_3 as a transmission line of some suitable characteristic impedance. The software was modified so that the unknown parameter X_3 was replaced by l_3, the length of the required feedback transmission line.

The design process then proceeds as follows.

1) The large-signal device S-parameters are modeled (or measured) at a selection of powers incident at both ports.

2) A value for $|V_1^+|$ is chosen. This fixes $S_{11}(|V_1^+|)$ and $S_{21}(|V_1^+|)$. A value of $|V_2^+|$ is estimated from expected gain considerations, and used to set $S_{12}(|V_2^+|)$ and $S_{22}(|V_2^+|)$.

3) A_{opt} is calculated from (13) using only the chosen device S-parameters; the ratio V_2^+/V_1^+ can then be found from (5), and the ratio $P/|V_1^+|^2$ from (10). All these quantities are independent of the device reference planes, i.e., of the transmission line lengths ultimately chosen. This enables the designer to check that the output S-parameters, $S_{12}(|V_2^+|)$ and $S_{22}(|V_2^+|)$, that were used correspond to those at the actual value of $|V_2^+|$ calculated. Furthermore, the oscillator output power, at the selected value of $|V_1^+|$, can now be calculated.

By varying the value of $|V_1^+|$ selected in step 2), a curve of output power versus incident input power (as done by Johnson [7] or Pucel [9]) may be generated. Each such output power is the maximum deliverable power to the load at the selected value of $|V_1^+|$.

4) The value of $|V_1^+|$ that gives the peak output power is used (with corresponding $|V_2^+|$) to set the S-parameters at the device operating point. The external element values are then found through solution of (6).

A large-signal model [7] was used to predict the S-parameters of the NEC 869177 FET employed in the construction of an oscillator, which operated near 5 GHz. This transistor has a nominal I_{DSS} of 330 mA, and a pinchoff voltage around 5 V.

Table I illustrates the steps in the design of the oscillator. The first column groups blocks of data according to the values of $|V_1^+|^2$ (incident input power) selected. The final line in each block, indicated by a check, is that for which the correct value of $|V_2^+|^2$ (incident power at the output) has been obtained. Thus in the first line of block 1, an incident input power of 17.7 dBm was chosen, and an incident output power of 19.9 dBm estimated. This estimate for the power incident on the output port might be based on a transistor with a gain of 6 dB, operating into a load reflection coefficient of 0.65. The S-parameters are thus defined since the incident powers are known, and step 3) of the design process can be performed. From (13), $A_{opt} = 2.77 + j1.56$; using this in (5) gives $|V_2^+|^2$ corresponding to 24.6 dBm. Since our first estimate of $|V_2^+|^2$ was only 19.9 dBm, the estimate of incident power at port 2 was increased in the second line of block 1, thus changing $S_{12}(|V_2^+|)$ and $S_{22}(|V_2^+|)$. After recalculation, the new incident output power is found to be close to that initially assumed. As shown, the magnitude of A is 2.27 in this case, and the ratio $P/|V_1^+|^2$, from (10), is 4.0, giving a predicted power of 235 mW delivered to the 50-Ω load, for the selected $|V_1^+|^2$ of 17.7 dBm. This is the maximum available power from the device under the chosen terminal conditions (i.e., for the given S-parameters used).

Cases 2), 3), and 4) show the results obtained by selecting higher values of incident input power. The output power does not continue to increase with $|V_1^+|^2$, but reaches a peak of 300 mW in cases 2) and 3). This is then the desired operating point. Case 2) was used rather than

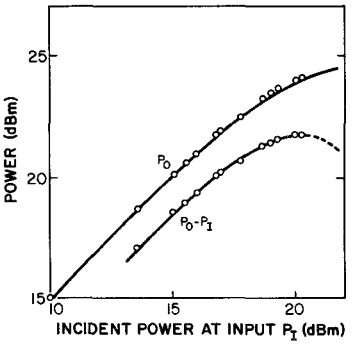

Fig. 3. Measured gain-saturation characteristics of the FET chip. The upper curve shows the output power as a function of the incident input power; the lower curve shows the net available power, which is the difference between the output and incident input powers. $V_{DS} = 7.5$ V, $V_{GS} = -3$ V.

TABLE I
DESIGN VALUES FOR 5-GHz OSCILLATOR

Case		$\lvert V_1^+\rvert^2$ (dBm)	$\lvert V_2^+\rvert^2$ (dBm) Est.	Calc.	A_{OPT}	$\frac{P_{LOAD}}{\lvert V_1^+\rvert^2}$	P_{LOAD} CALC. (mW)
1	x	17.7	19.9	24.6	2.77+j1.56	5.16	-
	√	17.7	21.2	20.9	2.07+j1.37	4.00	235
2	x	19.3	19.9	26.0	2.67+j1.54	4.86	-
	√	19.3	22.0	21.1	1.82+j1.35	3.52	300
3	x	20.7	26.4	16.4	.678+j1.45	2.05	-
	x	20.7	19.9	26.1	2.30+j1.36	3.55	-
	x	20.7	23.4	19.1	1.27+j1.24	2.28	-
	√	20.7	22.0	21.3	1.51+j1.25	2.55	300
4	x	22.0	23.4	19.3	.998+j1.17	1.61	-
	√	22.0	22.0	21.4	1.25+j1.15	1.82	288

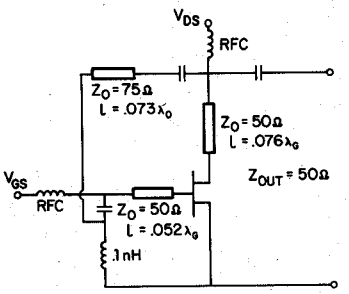

Fig. 4. Predicted oscillator circuit for maximum power output for the topology chosen. The blocking capacitors used were 100 pF.

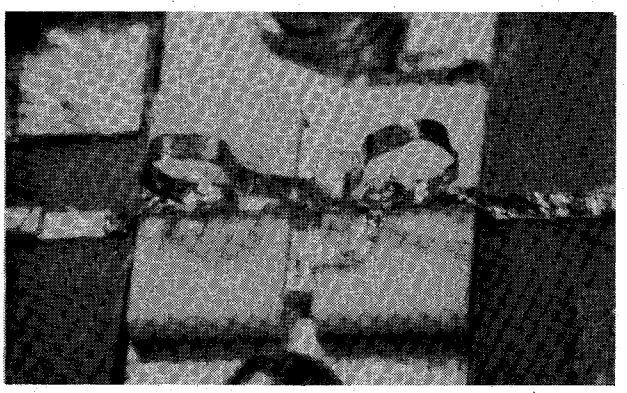

Fig. 5. Photograph of 5.35-GHz oscillator.

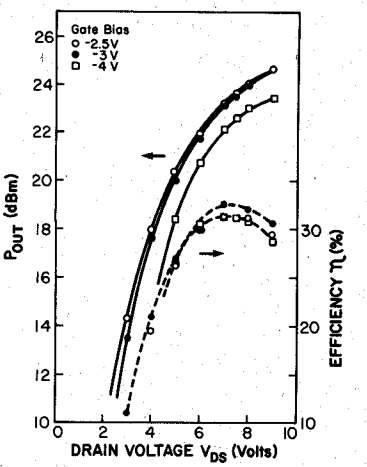

Fig. 6. Oscillator efficiency and output power.

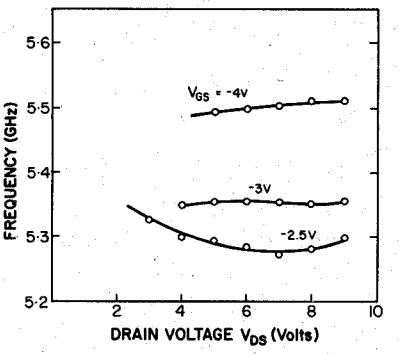

Fig. 7. Frequency pushing characteristics.

case 3) because of the better accuracy in the application of *S*-parameters at the lower input power level, since the FET is not saturated as much [3]. The reason for the peaking of output power can be seen in Fig. 3, which shows the measured gain-saturation characteristics of the unmatched transistor chip. The net available power from the device, $P_{out} - P_{in}$, shown by the lower curve, indicates that the available output power will peak for some value of incident power. The shape of this experimentally measured curve correlates well with the column labeled P_{load} in Table I, even though the matching conditions are different in the two cases.

The values of the *S*-parameters at this operating point are then used in a root finding routine to solve (6) for the network elements. The routine used was a standard IMSL FORTRAN routine, ZXMIN. It was found that convergence to a solution was highly dependent on the initial starting values, and that multiple solutions are possible. The approximate CPU cost of one design was ten cents.

The design attained was readily realizable, and is shown in Fig. 4. The driving point impedance of $-50\ \Omega$ was verified using a linear circuit analysis program.

The characteristic impedance of the feedback line was selected through realizability considerations. Doubling Z_0 of this line approximately halved its length, which made it too short to allow connection to the feedback points. This line was implemented through a piece of copper ribbon suspended close to the substrate. The gate inductance, which has a very high admittance (and hence can be thought of as the oscillator resonator), was implemented by a short piece of copper ribbon to ground. A photograph of the oscillator is shown in Fig. 5. The gate is on the right; the bias leads can be seen coming in at the edges of the picture; the feedback loop, shunt inductance, and chip capacitors are easily discernable.

VI. Results

The oscillator was operated with a gate bias of -3 V and drain voltage of 7.5 V. By slightly changing the length of the feedback loop, the frequency was adjusted to 5350 MHz. Without any tuning of the output, the power into the 50-Ω load was 23.4 dBm. By tuning around the output connector, the power increased to 23.9 dBm, compared with the predicted output power of 24.8 dBm. The efficiency obtained was 34.7 percent, which was the maximum over all operating points. Maximum power of 25 dBm was obtained by raising the drain voltage to 9.56 V.

Fig. 6 plots efficiency and power out as a function of drain and gate bias. Oscillations started at a drain voltage of 2.2 V and were observed for gate voltages higher than -4.4 V. It can be seen that even near peak power the efficiency is still very high. Fig. 7 shows the frequency pushing observed due to changes in the bias voltage. Sensitivity to gate voltage is about 150 MHz/V, while frequency is relatively insensitive to drain voltage variations. Although the oscillator was designed using *S*-parameters at a fixed gate bias of -3 V, oscillation was still achieved over a wide range of bias voltages, indicating the usefulness of *S*-parameters (which are relatively bias insensitive) in oscillator design.

Temperature variation in power and frequency at the

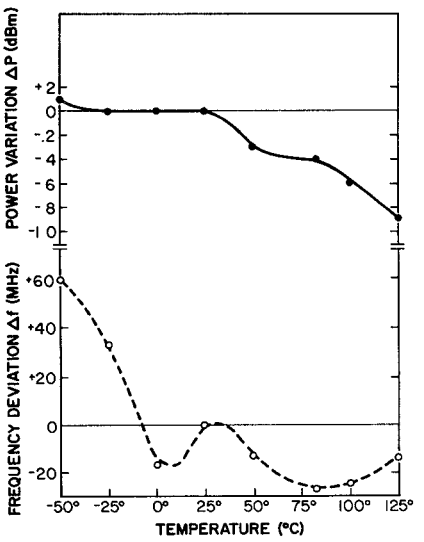

Fig. 8. Power and frequency variation with temperature.

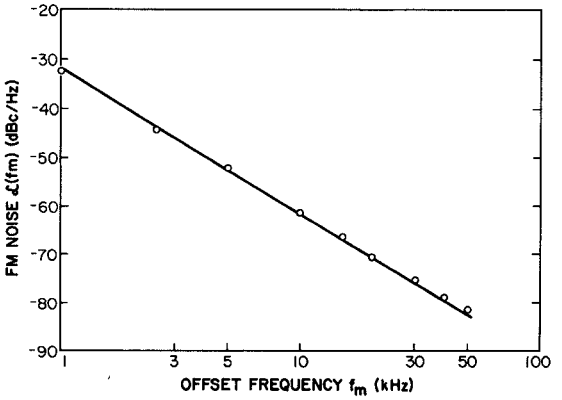

Fig. 9. Oscillator FM noise.

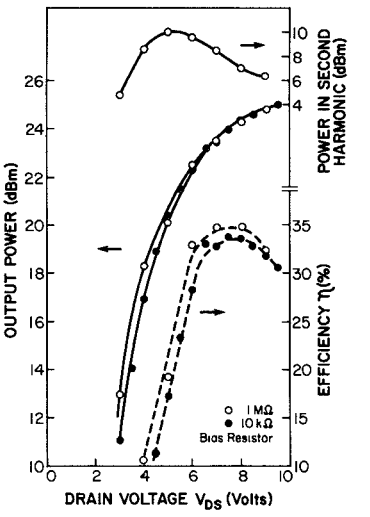

Fig. 10. Total power, second harmonic power, and efficiency in self-biased operation.

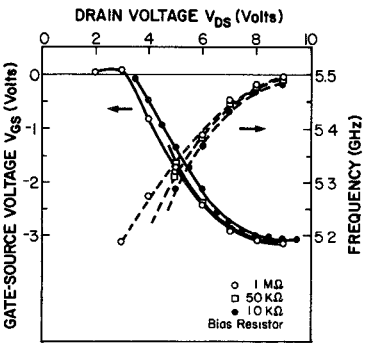

Fig. 11. Frequency and developed gate-bias in self-biased operation.

design point are plotted in Fig. 8. When the temperature was raised from −50°C to +125°C, the power decreased by 1 dB. The frequency dropped by 74 MHz, giving an average temperature sensitivity of −0.42 MHz/°C.

The frequency noise was measured in a 300-Hz bandwidth, from 1 kHz to 50 kHz off the carrier. The noise is plotted in decibels below the carrier in Fig. 9. The gate bias was held at −2.5 V, and the drain voltage at 9 V, corresponding to an output power of 24.9 dBm, close to peak power. The external Q of the oscillator was found to be 29 through load pull measurements (a sliding load with VSWR of 1.5 was varied over all phases; frequency pulling was 74 MHz). Because the noise measurements are within the resonator bandwidth, the FM noise slope was 30 dB/decade.

The oscillator was also operated in self-biased mode. As the drain voltage is raised, the drain current increases very rapidly at first until oscillation commences and a negative bias develops on the gate. Performance under these conditions was excellent, with peak power of 25 dBm being obtained at a drain voltage of 9.5 V, at an efficiency of 30.5 percent. Peak efficiency of 35 percent was achieved at an output power of 24 dBm. Because of the self-limiting oscillation process, harmonic power was high. However, at peak power the total harmonics were 18.4 dB down, although at lower powers the ratio was much higher. Output power, harmonic power, and efficiency are plotted in Fig. 10. The parameter is the external resistor used to develop the self bias. Fig. 11 presents the frequency and developed gate bias of the oscillator as a function of externally applied drain voltage. The frequency pushing is reasonably linear (+50 MHz/drain V). The oscillator could also be frequency modulated by varying the gate voltage.

Finally, to test the sensitivity of the design to the transistor S-parameters, a second NEC-869177 FET was inserted into an identical circuit. The I–V characteristics of this transistor were substantially different from the first (up to 30 percent higher drain current was observed at identical bias points). By tuning only the output connector on the drain, a slightly smaller output power of 22.7 dBm was obtained at the design bias point; the frequency was 5230 MHz. However, a much lower efficiency (22 percent) was recorded due to the substantially worse dc characteristics. In self-bias operation, a peak power of 24.2 dBm was obtained within the safe thermal limits of device operation.

VII. Conclusions

A systematic method has been presented for oscillator design using a GaAs MESFET. By analytic means, an embedding network can be derived which will deliver

specified power into a required load at a given frequency. The advantages of this approach are that it is a true two-port design method which requires no creation of an equivalent one-port circuit, the output load is directly specified, and power is automatically maximized for the device operating conditions. Thus, no computer optimization of the circuit is necessary. Furthermore, the device is completely described only by its large-signal S-parameters. No assumptions are required about the form of the nonlinearity in order to set the required load impedance for maximum power output as long as the device S-parameters have the required functional dependence to permit their definition under large-signal conditions.

A GaAs FET oscillator was built which verified the design approach. At 5.35 GHz, an output power of 245 mW was obtained with efficiency of 35 percent, using a 750-μm gate width FET. This technique may prove particularly valuable in the design of high-efficiency monolithic FET oscillators and power amplifiers.

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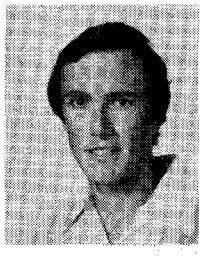

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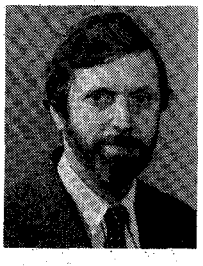

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